UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,474	10/27/2003	Christophe Pierrat	FTIS 1004-1	4270

22470 7590 02/16/2005

HAYNES BEFFEL & WOLFELD LLP
P O BOX 366
HALF MOON BAY, CA 94019

EXAMINER	
LIN, SUN J	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 02/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/694,474	PIERRAT ET AL.	
	Examiner	Art Unit	
	Sun J. Lin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 15-25* is/are rejected.

7)☒ Claim(s) *14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/27/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/27/03, 11/13/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/694,474 filed on 10/27/2003. Claims 1 – 25 remain pending in the application.

Claim Objections

2. Claims listed below are objected to because of the following informalities:

Claim 4, line 3, before "correction" insert —**proximity effect**—.
Claim 5, line 3, before "correction" insert —**proximity effect**—.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2, 4, 5, 12, 15 – 17, 18 and 20 – 24 are rejected under 35 U.S.C. 102(b) as being unpatentable over U.S. Patent No. 5,553,274 to *Liebmann*.

5. As to Claim 1, *Liebmann* shows and teaches the following subject matter:

- An *optical proximity correction (OPC) routine* on a mask layout pattern of a *VLSI* (i.e., *integrated circuit*) defined by a *computer aided design (CAD) (pattern layout) data* (i.e., *computer readable data file*) of a *lithography mask* to produce a *modified layout data set* (i.e., *corrected layout data file*) – [abstract; col. 6, line 41 – 49];
- Receiving a *polygon* from the *CAD pattern layout data* (*computer readable data file*), the polygon corresponding to a portion of the *VLSI* (*integrated circuit*) – [Fig. 3];
- Performing, using a *shapes processor means* (i.e., *data processor*), a *fracturing* (i.e., *fragmentation*) to *separate* the polygon into a set of *smaller*

fractured data pieces (i.e., *shapes*), based upon *parameters n, m* of a *photomask writer* (i.e., *manufacturing tool*) used for implementing the layout – [abstract; col. 6, line 61 – col. 7, line 11; Fig. 15; col. 5, line 61 – col. 6, line 50];

- Performing, using a shapes processor (data processor), a OPC on the *critical features* (i.e., *smaller shapes*) in the *fractured data pieces* to provide a *modified data set* (i.e., *corrected layout file*) – [abstract; col. 6, line 41 – 50];
- Providing the *modified data set* (*corrected layout file*) to the *mask writer* (*manufacturing tool*) – [col. 6, line 47 – 50].

For reference purposes, the explanations given above in response to Claim 1 are called **[Response A]** hereinafter.

6. As to Claims 17, 18 and 20 – 24, reasons are included in **[Response A]** given above.

7. As to Claim 2, reasons (*manufacturing tool* comprising a *mask writer*) are included in **[Response A]** given above.

8. As to Claims 4 and 5, *Liebmann* shows in Fig. 15 and teaches (1) during fracturing (fragmentation) procedure two parameters n, m are utilized (2) parameter n is the *minimum feature size* and parameter m is the *maximum feature size* – [col. 5, line 61 – col. 6, line 50; Fig. 15].

9. As to Claim 12, *Liebmann* shows and teaches the subject matter in Fig. 13. Notice that smaller shape 42 is a critical area of the layout.

10. As to Claims 15 and 16, *Liebmann* shows and teaches the subject matter in Fig. 13. Notice that polygon including shapes 42 and 44 is the *first polygon*; whereas polygon including shapes 45 and 43 is the *second polygon*. The *second polygon* is fractured (fragmented), and shape 43 is a corner of the *second polygon*.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

(1). Determining the scope and contents of the prior art.
(2). Ascertaining the differences between the prior art and the claims at issue.
(3). Resolving the level of ordinary skill in the pertinent art.
(4). Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. Claims 3, 13, 19 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,553,274 to *Liebmann* in view of U.S. Patent No. 4,475,037 to *Vettiger et al.*

13. As to Claims 3 and 13, in addition to subject matter regarding to *manufacturing tool* comprising a *mask writer* as explained in [Response A] given above, *Liebmann* also discloses using *e-beam* (tool) in *writing photo masks* and in direct wafer writing operations – [col. 1, line 51 – 63]. *Liebmann* does not teach *vector scan e-beam tool*. But *Vettiger et al.* teach an *electron beam (i.e., e-beam) vector scan system* for use in inspecting an *e-beam fabricated mask* – [title; abstract]. *Vettiger et al.* also teach that an e-beam vector scan system is utilized in order to *inspect the e-beam fabricated mask* thereby precisely detecting pattern coincidence or non-coincidence of the desired e-beam pattern to eliminate false defect and to enhance the true defects – [abstract; col. 2, line 42 – 62].

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Vettiger et al.* in utilizing an *e-beam vector scan system* is in inspect the *e-beam fabricated mask* in

order to precisely detect pattern coincidence or non-coincidence of the desired e-beam pattern to eliminate false defect and to enhance the true defects.

Vettiger et al. also teach *scaling* the *system parameters* (*size*, *orthogonality* etc.) of the *e-beam vector scan system* – [col. 4, line 15 – 22]. Notice that the size parameters comprise scanning dimensions, which need to be scaled appropriately in order to effectively overlay the printed mask pattern with a virtual one written when the system is instruct to write.

14. As to Claim 19, in addition to subject matter regarding to *manufacturing tool* comprising a *mask writer* as explained in **[Response A]** given above, *Liebmann* also discloses using *e-beam* (tool) in *writing photo masks* and in direct wafer writing operations – [col. 1, line 51 – 63]. *Liebmann* does not teach *vector scan e-beam tool*. But *Vettiger et al.* teach an *electron beam (i.e., e-beam) vector scan system* for use in *manufacturing* and *inspecting* a photo mask – [title; abstract; col. 3, line 16 – 36].

Vettiger et al. also teach (1) exposing a mask blank coated with an *e-beam sensitive resist* (e.g., *high contrast (to electrons) material*) – [col. 3, line 23 – 27] (2) scaling *system parameters* to those of wafer such as size, orthogonality etc., *vector scan system* will effectively overlay the printed mask pattern with a virtual one written when the system is instructed to write – [col. 4, line 15 – 22]. Notice that *system parameter* is scaled in order to accurately and effectively expose the shapes representing the critical dimensions of the layout on the mask.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Vettiger et al.* in utilizing an *e-beam vector scan system* by exposing mask blank coated with an high e-beam sensitive resist and scaling the system parameter of the *e-beam vector scan system* in order to accurately and effectively expose the shapes representing the critical dimensions of the layout on the mask.

For reference purposes, the explanations given above in response to Claim 19 are called **[Response B]** hereinafter.

15. As to Claim 25, reasons are included in [Response B] given above.

16. Claims 6 – 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,553,274 to *Liebmann* in view of U.S. Patent Application Publication No. 2004/0052411 A1 to *Qian et al.*

17. As to Claims 6 – 9, as explained in **[Response A]**, *Liebmann* teaches providing a *modified data set* (*corrected layout file*) to the *mask writer* for use in correcting patterns in lithography for *critical features* using OPC technique. *Liebmann* does not teach providing a *modified data set* (*corrected layout file*) to the *mask writer* for to make a *binary mask*, an *attenuated phase-shifting mask*, a *tri-tone phase-shifting mask* and *alternating aperture phase-shifting mask* for correct critical features in lithography process. But *Qian et al.* teach using *binary mask*, an *attenuated phase-shifting mask*, a *tri-tone phase-shifting mask* and *alternating aperture phase-shifting mask* in order to improve printability ultra-small IC features below 0.18 μm in lithography process of a wafer pattern – [paragraph 0006, 0008, 0022, and 0023].

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Liebmann* and *Qian et al.* in providing a correct layout file for use in making a *binary mask*, an *attenuated phase-shifting mask*, a *tri-tone phase-shifting mask* or an *alternating aperture phase-shifting mask* in order to improve printability of ultra-small IC features below 0.18 μm in lithography process of a wafer pattern of an submicron integrated circuit.

18. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,553,274 to *Liebmann* and U.S. Patent Application Publication No. 2004/0052411 A1 to *Qian et al.* in view of Paper entitled "*Hierarchical Processing of Levenson-Type Phase Shifter Generation*" to *Yamamoto et al.*

19. As to Claim 10, *Qian et al.* teach positions and phase relations (e.g., 180° out of phase) between two adjacent *phase shifters* (i.e., *phase-shifting regions*) in an

(alternating) phase-shifting mask (AtlPSM) for a critical feature – [Paragraph 0008, 0022]. *Qian et al.* do not teach *storing phase information* of the *phase shifters*. But *Yamamoto et al.* teach *storage of phase information* of phase shifter – [Paragraph 2.2 Phase Information; Fig. 2]. *Yamamoto et al.* also teach that phase information is stored as a combination of two properties, phase and group reversal in order to keep CAD data compressed during *phase assignment* in implementation of AtlPSM – [abstract]

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Yamamoto et al.* in storing phase information as a combination of two properties, phase and group reversal in order to keep CAD data compressed during phase assignment in implementation of AtlPSM.

20. As to Claim 11, it is inherent that the *(phase) information* about the two adjacent edges (phase shifters), which are always 180° out of phase, is used to facilitate the phase assignment of the phase shifter (phase-shifting regions).

Allowable Subject Matter

21. Claim 14 is objected to as being dependent upon a rejected base claim, but it would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Those claims are allowed is because that the prior art does not teach or fairly suggest the following subject matter:

- A method for performing proximity effect correction on a layout of an integrated circuit comprising performing a proximity effect correction on a smaller shape in a set of smaller shapes in a fragmented polygon corresponding to a portion of the integrated circuit wherein a boundary between adjacent shapes in the set of smaller shapes is adjusted to account for a position of an edge of at least one of the adjacent shapes which is modified by the proximity effect correction in combination with other limitations as recited in **Claim 14**.

Conclusion

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J Lin whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday 9:30AM - 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (571) 272 - 1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sun James Lin
Patent Examiner
Art Unit 2825
February 14, 2005